Department of Electrical Engineering and Computer Science
Ohio University, Athens, Ohio.

Course Syllabus
Fall 2022 EE 6900: Interconnection Networks for High-Performance Computing (HPC) Systems & Accelerators

Course Information

Class Number: 14052
Section: 100
Credits: 3
Days: MWF
Time: 12:55 PM - 1:50 PM
Location: ARC 108
Webpage: http://ace.cs.ohio.edu/~avinashk/classes/ee690/ee690.htm

Course Instructor Information

Name: Avinash Karanth
Rm: STKR 335
Phone: (740)-597-1481
E-mail: karanth@ohio.edu
Office Hours: 10:00 AM - 12:00 PM Wednesday or via MS Teams

Textbook

- (Optional) Computer Architecture: A Quantitative Approach, 4th Edition, Appendix E.
- (Optional) Interconnection Networks: An Engineering Approach By Jos Duato, Sudhakar Yalamanchili, Lionel M. Ni
- (Optional) Principles and Practices of Interconnection Networks by William Dally and Brian Towles.

Prerequisites

- EE 3613: Computer Organization (or any basic computer architecture course)

Class Policies

- *COVID-19 Policies*: If you do test positive or need to isolate or quarantine this semester, after you have taken care of yourself and followed all the steps in the OHIO COVID-19 Protocol, please email me so that we can develop a plan for you to receive the necessary course content. COVID-related illness, quarantine, isolation, and remain-in-room directives are legitimate university absences, and I will work with you to manage your academic requirements and connect you to resources. If you feel that your class performance is being impacted by COVID-19, please talk with me and/or contact Public Health Operations by email (PHO@ohio.edu). The University has information about resources available to help with quarantine and isolation here (https://www.ohio.edu/coronavirus/protocol)

- *Accommodation*: Any student who feels they may need an accommodation based on the impact of a disability should contact me privately to discuss your specific needs and provide written documentation from Student Accessibility Services. If you are not yet registered as a student with a disability, please contact Student Accessibility Services at 740-593-2620 or visit the office in 348 Baker University Center.
- *Course Material:* All course material will be made available at the website noted above. The weblink will be made available via Blackboard as well.
- *Attendance*: Class attendance is strongly encouraged. I will do my best to post upcoming lecture topics. Check the class webpage regularly for announcements on lectures, assignments and paper readings.
- *Academic Misconduct*: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Please refer to the OU Student Code of Conduct.
- *Assignments*: Assignments are due on Blackboard on the date and time specified. **All homework and term paper are to be done individually**.
- *Regrades*: All requests for regrades must be submitted within one week of the distribution of the graded material.
- *Exams*: Exams will be conducted in-class. Precise instructions will be provided before each exam.
- *Grades*: All grades will be posted on Blackboard. All grading is based on the 12-point system. [100-93] A, [92-90] A-, [89-87] B+, [86-83] B, [82-80] B-, [79-77] C+, [76-73] C, [72-70] C-, [69-67] D+, [66-63] D, [62-60] D-, [59-..] F. Instructor reserves the right to lower the limits above, but I promise not to raise them.

Grading Policy

Homeworks (4): 20%
Midterms (2): 40%
Presentation: 20%
Term Paper: 20%

Course Outline

EE 6900 is intended to provide graduate students with an in-depth study of interconnection networks for high-performance computing (HPC) systems, multi-cores and hardware accelerators. Interconnection networks offer an attractive and economical solution to this communication crisis and are fast becoming pervasive at all levels of digital system, whether it be on-chip, inter-chip, inter-board and inter-rack. As machine learning based accelerators begin to dominate the market, this course will also analyze the impact of data movement for deep learning applications. Emerging technologies such as photonics and wireless will also be discussed. Topics covered include:
[1] Introduction to Interconnection Networks
[2] Topology
[3] Switching Techniques

[4] Taxonomy of Routing Algorithms
[5] Flow Control
[6] Router Micro-architecture
[7] Hardware Accelerators.

Course Outcomes

In-depth understanding of the design and engineering of interconnection networks

- Ability to understand the working of interconnection networks at on-chip and off-chip levels
- Ability to understand techniques for designing various network/interconnect topologies
- Ability to differentiate between various switching and routing techniques
- Ability to understand various flow control techniques implemented by interconnection networks
- Ability to understand the working of the router microarchitecture
- Ability to evaluate future technologies for implementing the interconnection network

Tool

- YACSIM/NETSIM - a discrete event simulator for network simulation.

Tentative Dates

Midterm-1: Monday October 3, 2022 (in-class)
Midterm-2: Monday November 21, 2022 (via Proctortrack)
Presentations: Last week of classes (Nov 28 - Dec 2)
Term Paper: Friday December 9, 2022